NONVOLATILE MEMORY WITH SPACER TRAPPING STRUCTURE

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device, and more specifically, to a nonvolatile memory with spacer structure capable of trapping carriers.

BACKGROUND

[0002] The semiconductor industry has been advanced to the field of Ultra Large Scale Integrated Circuit (ULSI) technologies. The fabrication of the nonvolatile memories also follows the trend of the reduction in the size of a device. The nonvolatile memories include various types of devices. Different types of devices have been developed for specific applications' requirements in each of these segments. Flash memory is one of the segments of nonvolatile memory devices. The device includes a floating gate to storage charges and an element for electrically placing charge in and removing the charges from the floating gate. One of the applications of flash memory is BIOS for computers. Typically, the high-density nonvolatile memories can be applied as the mass storage of portable handy terminals, solid-state camera and PC cards. It is because that the nonvolatile memories exhibit many advantages, such as memory retention without power, fast access time, low power dissipation in operation, and robustness.

[0003] The formation of nonvolatile memories toward the trends of low supply power and fast access, because these requirements are necessary for the application of the mobile computing system. Nonvolatile memory needs the charges to be hold in the floating gate for a long period of time. Therefore, the dielectric that is used for insulating the floating gate needs to be high quality in insulation and good durability in writing. At present, the flash memories use

tunneling effect or hot carrier effect to charging or discharging the floating gate. As known in the art, the tunneling effect is a basic technology in charging or discharging. In order to attain high tunneling efficiency, the thickness of the dielectric between the floating gate and substrate have to be scaled down due to the supply voltage is reduced. A high voltage is applied to a control gate to induce a high electric field in a tunnel oxide layer, and electrons of a semiconductor substrate pass the tunnel oxide layer and are injected into a floating gate. During the mode of erasing, the bias may apply on the source to discharge the electron from the floating gate to the source of a memory device.

[0004] Currently, the SOC (system on chip) desires memory with high operation speed and integrated in one single chip. For example, the single polysilicon processing may integrate with other devices such as transistors. The typical non-volatile memory employs stack gate memories by double polysilicon processing. One type of the memories uses trapping layer instead of floating gate (FG) to hold the carrier. The memory cells are constructed with a trapping ONO layer. A nitride layer sandwiched between two oxide layers and a polycrystalline layer. To program or write the cell, voltages are applied to the drain and the gate and the source is grounded. These voltages generate an electric field along the length of the channel from the source to the drain. This electric field causes electrons to be drawn off the source and begin accelerating towards the drain. The hot electrons are generated at the boundary between drain and channel during the acceleration.

[0005] In the prior art, please refer to U.S. Patent No. 4,881,108, U.S. Patent No. 5,768,192 to Eitan B. entitled "Non-volatile semiconductor memory cell utilizing asymmetrical charge trapping", filed on 16 June, 1998. The charge trapping memory may also be referred to U.S. Patent No. 6,335,554 to Yoshikawau and Kuniyoshi, entitled "Semiconductor Memory". The patent disclosed a memory with ONO structure. Further article teaches the memory with ONO stacked layer could also be found, please refer to the article, Chan, T.Y. et al, "A True Single-

Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, vol. EDL-8. No. 3, Mar. 1987 ◦

SUMMARY

[0006] The object of the present invention is to disclose a nonvolatile memory with spacer structure capable of trapping carriers.

[0007] The present invention discloses a nonvolatile memory with spacer trapping structure, the nonvolatile memory comprising a semiconductor substrate. A gate oxide is formed on the semiconductor substrate. A gate structure is formed on the gate oxide. An isolation layer is formed on the sidewall of the gate structure. First spacers are formed on the sidewall of the isolation layer for storing carriers and source and drain regions formed adjacent to the gate structure. And the p-n junctions of source and drain regions are located under the spacer structure. Salicide is formed on the gate structure and the source and drain regions.

[0008] The nonvolatile memory further comprises pocket ion implantation region located adjacent to the source and drain regions and under the spacer structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions. Alternatively, the nonvolatile memory further includes lightly doped drain region adjacent to the source and drain regions, wherein the junction of the lightly doped drain region is under the spacer structure and shallower than the one of the source and drain regions and the lightly doped drain region is closer to the channel under the gate structure than the source and drain regions; and pocket ion implantation region adjacent to the source and drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions. Further embodiment, the nonvolatile memory further comprises double doped drain region adjacent to the source and drain regions, wherein the junction of the double doped drain region is under the spacer structure and deeper than the one of the source and drain regions and the double doped drain region is closer to the channel under the gate structure than the source and drain regions; and pocket

ion implantation region adjacent to the double doped drain region and under the undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[0009] The first spacer includes nitride or the materials having energy gap lower than 6eV. The present invention may further include second spacers attached on the first spacers, wherein the second spacers are formed of oxide or the material having energy gap larger than 7eV. The isolation layer is formed of oxide or the material having energy gap larger than 7eV. Wherein the silicide material includes $TiSi_2$, WSi2, $CoSi_2$ or NiSi.

[0010] The present invention discloses a nonvolatile memory with spacer trapping structure, the nonvolatile memory comprising a semiconductor substrate; a gate oxide formed on the semiconductor substrate. A gate structure is formed on the gate oxide, wherein the gate structure comprises a stacked structure including polysilsicon layer/silicide layer and a first dielectric layer. A second dielectric layer is formed over the sidewall of the gate structure. First spacers are formed on the sidewall of the second dielectric layer for storing carrier and source and drain regions formed adjacent to the gate structure. And the p-n junctions of source and drain regions are located under the spacer structure.

[0011] The present invention further comprises pocket ion implantation region located adjacent to the source and drain regions and under the spacer structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions. Alternatively, the nonvolatile memory further comprises lightly doped drain region adjacent to the source and drain regions, wherein the junction of the lightly doped drain region is under the spacer structure and shallower than the one of the source and drain regions and the light doped drain region is closer to the channel under the gate structure than the source and drain regions; and pocket ion implantation region adjacent to the source and drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions. In another preferred embodiment, the present invention further comprises double

doped drain region adjacent to the source and drain regions, wherein the junction of the double doped drain region is under the spacer structure and deeper than the one of the source and drain regions and the double doped drain region is closer to the channel under the gate structure than the source and drain regions; and pocket ion implantation region adjacent to the double doped drain region and under the spacer structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[0012] Wherein the first spacer includes nitride or the material has energy gap lower than 6eV. The nonvolatile memory may further comprise second spacers attached on the first spacers, wherein the second spacers are formed of oxide or the material having energy gap larger than 7eV. The second dielectric layer later is formed of oxide or the material having energy gap larger than 7eV. The first spacers are formed of nitride or the material having energy gap lower than 6eV. The silicide material includes $TiSi_2$, $CoSi_2$ or NiSi. Further, the first dielectric layer is formed of oxide or nitride or the combination of oxide and nitride layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0014] FIGURE 1 is a cross sectional view of a semiconductor wafer illustrating the first embodiment according to the present invention.

[0015] FIGURE 2 is a cross sectional view of a semiconductor wafer illustrating the second embodiment according to the present invention.

[0016] FIGURE 3 is a cross sectional view of a semiconductor wafer illustrating the third embodiment according to the present invention.

[0017] FIGURE 4 is a cross sectional view of a semiconductor wafer illustrating the forth embodiment according to the present invention.

[0018] FIGURE 5 is a cross sectional view of a semiconductor wafer illustrating the fifth embodiment according to the present invention.

[0019] FIGURE 6 is a cross sectional view of a semiconductor wafer illustrating the sixth embodiment according to the present invention.

[0020] FIGURE 7 is a cross sectional view of a semiconductor wafer illustrating the seventh embodiment according to the present invention.

[0021] FIGURE 8 is a cross sectional view of a semiconductor wafer illustrating the eighth embodiment according to the present invention.

[0022] FIGURE 9 is a cross sectional view of a semiconductor wafer illustrating the ninth embodiment according to the present invention.

[0023] FIGURE 10 is a cross sectional view of a semiconductor wafer illustrating the tenth embodiment according to the present invention.

[0024] FIGURE 11 is a cross sectional view of a semiconductor wafer illustrating the eleventh embodiment according to the present invention.

[0025] FIGURE 12 is a cross sectional view of a semiconductor wafer illustrating the twelfth embodiment according to the present invention.

[0026] FIGURE 13 is a cross sectional view of a semiconductor wafer illustrating the thirteenth t embodiment according to the present invention.

[0027] FIGURE 14 is a cross sectional view of a semiconductor wafer illustrating the fourteenth embodiment according to the present invention.

[0028] FIGURE 15 is a cross sectional view of a semiconductor wafer illustrating the fifteenth embodiment according to the present invention.

[0029] FIGURE 16 is a cross sectional view of a semiconductor wafer illustrating the sixteenth embodiment according to the present invention.

[0030] FIGURE 17 is a cross sectional view of a semiconductor wafer illustrating the seventeenth embodiment according to the present invention.

[0031] FIGURE 18 is a cross sectional view of a semiconductor wafer illustrating the eighteenth embodiment according to the present invention.

[0032] FIGURE 19 is a cross sectional view of a semiconductor wafer illustrating the nineteenth embodiment according to the present invention.

[0033] FIGURE 20 is a cross sectional view of a semiconductor wafer illustrating the twentieth embodiment according to the present invention.

[0034] FIGURE 21 is a cross sectional view of a semiconductor wafer illustrating the twenty-first embodiment according to the present invention.

[0035] FIGURE 22 is a cross sectional view of a semiconductor wafer illustrating the twenty-second embodiment according to the present invention.

[0036] FIGURE 23 is a cross sectional view of a semiconductor wafer illustrating the twenty-third embodiment according to the present invention.

[0037] FIGURE 24 is a cross sectional view of a semiconductor wafer illustrating the twenty-fourth embodiment according to the present invention.

DETAILED DESCRIPTION

[0038] The present invention proposes a novel structure for charge trapping nonvolatile memory. In the structure, the cell capacity for storing data can be increased by the cell structure. The detail description will be seen as follows. A semiconductor substrate is provided for the present invention. In a preferred embodiment, as shown in the FIGURE 1, a single crystal silicon substrate 2 with a <100> or <111> crystallographic orientation is provided. The substrate 2 includes a pattern of active areas. The isolation to separate the devices includes STI or FOX. A thin dielectric layer 4 consisted of silicon dioxide is formed on the substrate 2 to act as gate oxide. Typically, the layer 4 can be grown in oxygen ambient at a temperature of about 700 to 1100 degrees centigrade. Other method, such as chemical vapor deposition, can also form the oxide. In the embodiment, the thickness of the silicon dioxide layer 4 is approximately 15-250 angstroms. Subsequently, a conductive layer 6 is formed on the layer 4. The conductive layer 4 may be formed of doped polysilicon, in-situ doped polysilicon or epitaxy silicon. For an embodiment, the doped polysilicon layer 6 is doped by phosphorus using a PH_3 source. A photo-resist defined patterning process is used on the conductive layer 6, thereby forming the gate structure on the silicon substrate 2. It has to be noted that the gate structure includes a charge trapping

region 8 located at lower portion of the spacer 12 adjacent to the gate 6. Please refer to FIGURE 1, an isolation layer 10 is conformally formed on the substrate 2 and the gate structure 6. The material for forming the isolation layer 10 can be oxide (SiO_2) or (HfO_2) or the material with energy gap higher than 7 eV. One suitable method for the oxide layer 10 includes thermal oxidation and deposition by CVD. For example, Low Pressure Chemical Vapor Deposition (LPCVD), Plasma Enhance Chemical Vapor Deposition (PECVD), High Density Plasma Chemical Vapor Deposition (HDPCVD). Still referring to FIGURE 1, an isotropic etching is performed to create sidewall spacers 12 on the sidewall of the isolation layer 10. Reactive ion etching (RIE) or plasma etching is the typical way to achieve the purpose. The spacers 12 includes the charge trapping region 8, thereby forming the ON structure capable of trapping carriers to define the digital states. The material for the spacer could be nitride or the material with energy gap smaller than 6 eV. In the preferred embodiment, the reaction gases of the step to form silicon nitride layer include, for example, SiH4, NH3N2, N2O or SiH2Cl2, NH3N2,N2O

[0039] Turning to FIGURE 1, the p-n junction of source and drain region 14 is formed by performing an ion implantation to dope ions into the substrate 2 using the gate structure 6 and sidewall spacers 12 as a mask. After selectively etching isolation layer 10, portions of the gate 6 and substrate 2 are exposed. Silicide 16 is introduced on the exposed surface of the top portion of gate and the silicon substrate 2 on the source and drain regions 14 to reduce their resistance. Preferably, the silicide 16 can be $TiSi_2$, WSi_2, $CoSi_2$ or NiSi. The gate structure 6 acts as the control gate, and the nitride spacers are used to trap carriers. The spacers 12 are used to store charges, thereby defining the digital states including (0, 0), (0, 1), (1, 0), (1, 1). A sectional view of a multi-bit nonvolatile memory cell in accordance with the present invention is shown in FIG. 1-24. The memory cell includes a substrate 2 having at least two buried PN junctions, one is the left junction and the other is the right junction. Channels are located between the two junctions during operation. Above the main channel is an oxide 4, on top of the

oxide layer 4 is a control gate 6. Spacer 12 is used for charge trapping and is preferably comprised of silicon nitride. The hot electrons or holes are trapped as they are injected into the Spacer 12.

[0040] The memory cell is capable of storing two bits of data, a right bit and a left bit. The two bit memory cell is a symmetrical device. The left junction serves as the source terminal and the right junction serves as the drain terminal for the right bit programming. Similarly, for the left bit programming, the right junction serves as the source terminal and the left junction serves as the drain terminal. When the distinction between left and right bits is not crucial to the particular discussion, the terms source and drain are utilized as conventional manner.

[0041] Figure 2 illustrates the second embodiment of the present invention. Most of the parts are similar to the first embodiment, the difference between both includes that the example omits the salicide 16 at source and drain regions in the second embodiment. The gate is consisted of polysilicon 6a, silicide 6b and dielectric layer 6c. The silicide 6b is preferably formed of $TiSi_2$, WSi_2, $CoSi_2$ or NiSi. The dielectric layer 6c is formed of oxide, nitride or the combinations of oxide and nitride layers. The portion 8 of the trapping spacer 12 is used to trapping charge.

[0042] Turning to figure 3, the embodiment includes pocket ion implantation region 18 adjacent to the source and drain region 14 and adjacent to the gate structure to reduce the short channel effect and increase the efficiency of the hot carrier injection. Figure 4 shows the alterative example for the present invention, it is similar to the second embodiment. It also includes pocket ion implantation region 18 adjacent to the source and drain region 14. The conductive type of the pocket implant region 18 is opposite to the one of the source and drain region 14.

[0043] Figures 5 and 6 are the alternative approaches with respect to the embodiments shown in figures 3 and 4. The fifth and sixth embodiments introduce the lightly doped drain to control the hot carriers and further comprise pocket ion implant region 18 adjacent to the source and drain region 14 and under the portion 8 of the charge trapping spacers 12. The conductive type of the

pocket ion implantation region is opposite to the one of the source and drain region. The junction of the lightly doped drain is shallower than the one of the source and drain region. The lightly doped drain is also closer to the channel under the gate. Alternatively, the other embodiments shown in figures 7 and 8 introduce the usage of double diffused drain (DDD) structure to reduce the junction breakdown effect. The conductive ion type of the DDD structure is the same as that of the source and drain region. However, the junctions of the lightly doped regions are deeper than the junctions of the heavily doped source and drain region. The embodiments further comprise pocket ion implant region adjacent to the double diffused source and drain region and under the spacer structure 8 of the control gate 6.

[0044] Please refer to figure 9, the example is similar to the first embodiment except the spacer 12 is formed of oxide and in the ninth embodiment, there are double isolation layers formed on the gate structure 6 prior to the formation of the oxide spacer 12. The first isolation layer 10 is formed of oxide or the material with energy gap greater than 7 eV, and the second one 11 is formed of nitride or the material with energy gap smaller than 6 eV. Similarly, the preferred embodiments from figure 10-16 are the alternative solutions for the corresponding examples from figure 2-8. The spacers 12 are formed of oxide and the corresponding structures, features are very similar to those corresponding examples. The charge is also trapped by the nitride trapping layer. Therefore, the description is omitted.

[0045] Next, the embodiments shown in figure 17-24 are the alternative arrangements that are associated with figures 9-16, correspondingly. The main different is that the double-spacers structure is introduced into the embodiments shown in figure 17-24. The material for the fist spacer 12 is oxide. The ONO structure is consisted of the oxide layer 10, nitride layer 11 and the oxide spacer 12. The second spacer 13 is attached on the first spacer 12, the second spacer can be formed of oxide, nitride or the material having energy gap larger than 4 eV. The configuration, therefore, constructs the double spacers structure.

[0046] In the illustrations of the present invention, form the direction parallel to the surface of the paper, two spacers are located adjacent to the gate, hence, two-bits may be stored in the two nitride spacers, and other two bits could be stored in the two further nitride spacers, the two nitride spacers (not shown in the figures) could be observed from the direction perpendicular to the surface of the paper. Therefore, the present invention provides a multi-bit device for storing multi-bits digital signal. The trapping layer is formed of ONO or ON configuration to trap the carrier, thereby defining the digital states.

[0047] As will be understood by persons skilled in the art, the foregoing preferred embodiment of the present invention is illustrative of the present invention rather than limiting the present invention. Having described the invention in connection with a preferred embodiment, modification will now suggest itself to those skilled in the art. Thus, the invention is not to be limited to this embodiment, but rather the invention is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures. While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.